A Nonlinear Capacitance Cancellation Technique and its Application to a CMOS Class AB Power Amplifier

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Abstract: A nonlinear cancellation technique is developed specifically for MOS Class AB power amplifiers. This technique utilizes a PMOS transistor at the amplifier input to cancel the variation of the input capacitance, thus improving the overall amplifier linearity. A monolithic CMOS RF power amplifier with this technique is designed and fabricated in a standard $0.6\mu m$ CMOS technology. The prototype single-stage amplifier has a measured drain efficiency of 40% and a power gain of 7dB at 1.9GHz. Linearity measurements show that the new amplifier has over 10dB of IM_3 improvement and 6dB of ACPR improvement compared with the traditional NMOS Class AB power amplifier.

I. Introduction

RF power amplifiers traditionally consist of discrete Gallium Arsenide transistors assembled on hybrid modules. Although these power amplifiers can provide good performance, they are costly to manufacture and have a large printed circuit board footprint. In recent years, lower cost monolithic power amplifiers have been introduced[1]-[3]. Among them, monolithic MOS power amplifiers recieved more and more attention for their low cost and potential for high density and functionality[1][2].

Monolithic MOS power amplifiers capable of delivering 1W of RF power or more at 800-900Mhz were implemented in CMOS[1], LDMOS and BiCMOS[2]. However, those designs were intended for constant-amplitude applications and were intrinsically very nonlinear. Although several linearization techniques[4]-[6] are available to linearize nonlinear amplifiers, most of them are complicated and are not applicable to handset applications. Class AB power amplifiers are widely used in wireless trancievers for their simplicity and relatively high efficiency. However, the nonlinearity associated with Class AB amplifiers can seriously degrade the performance of the whole wireless system. In this paper, we propose a nonlinear capacitor cancellation technique to cancel the nonlinear input capacitance of the amplifier, thus improving the large-signal Class-AB linearity. A detailed analysis and a brief description of simulation and experimental results are presented in the following sections.

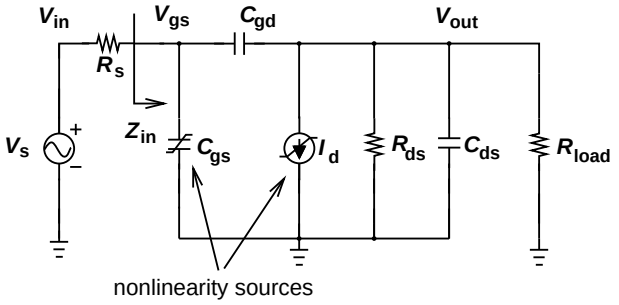

Fig. 1. Nonlinear model of NMOS Class AB power amplifier

II. Nonlinear Capacitor Cancellation

In a typical Class AB operation, the input signal is large enough to constantly turns device "on" and "off", causing "clipping" of the drain current. During this "clipping", two main sources of nonlinearity are created, as shown in Fig. 1. The first is the nonlinear input impedance Z_{in} seen by the input signal source V_s . When the transistor turns on and off, the gate capacitance C_{gs} changes dramatically. For a $0.6\mu m$ technology, C_{gs} changes from approximately 1pF/mm to almost 0pF/mm, while C_{gd} is almost unchanged. Assuming that C_{gd} is much less than C_{gs} and ignoring gate resistance, the input impedance of the amplifier is approximately:

$$Z_{in} = \frac{1}{j\omega C_{in}} = \frac{1}{j\omega(C_{gs} + (1+A)C_{gd})} \qquad (1)$$

Where A is the voltage gain of the amplifier. V_{gs} and V_{in} are related by:

$$V_{gs} = \frac{Z_{in}}{Z_s + Z_{in}} V_{in} \qquad (2)$$

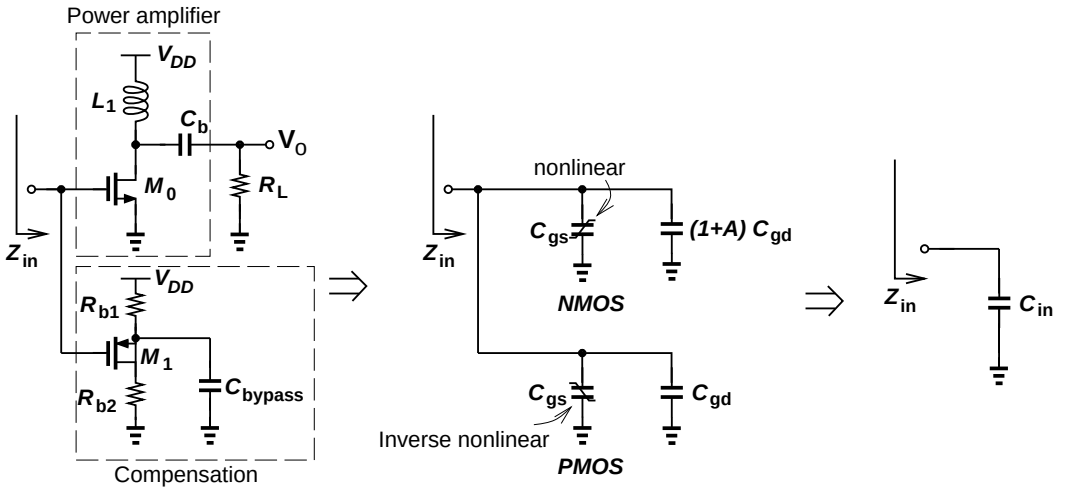

Fig. 2. Input capacitance after compensation

For linear amplification, V_{gs} should be a linear, delayed version of V_{in} , i.e.

$$V_{gs}\left(t\right) = CV_{in}\left(t - t_0\right) \tag{3}$$

Because Z_{in} is not a constant during Class AB operation, V_{gs} will be a "distorted" version of V_{in} , and create significant nonlinearity.

This nonlinearity can be reduced by introducing a parallel inverse nonlinearity at the input of the amplifier. If the two nonlinearities are well matched, the resulting input impedance will be very linear. This can be accomplished in CMOS technology through the use of a parallel PMOS device along with the NMOS gate; the PMOS device is biased so that when the NMOS device is "off", it turns the PMOS device "on" and contributes some capacitance. So no matter what state the transistor is in, the input capacitance is always approximately constant. Fig. 2 shows how this nonlinear cancellation works. By connecting the drain and source of the PMOS transistor together, only capacitive current flows into the PMOS transistor. The disadvantage of this technique is that the input capacitance will be larger than the original input capacitance, reducing the achievable power gain. The reduction in power gain depends on the working mode of the amplifier. If the NMOS device spends only a small portion of its cycle in the "off" state, C_{gs} is "on" for most of the time and the compensation network has little effect on the gain.

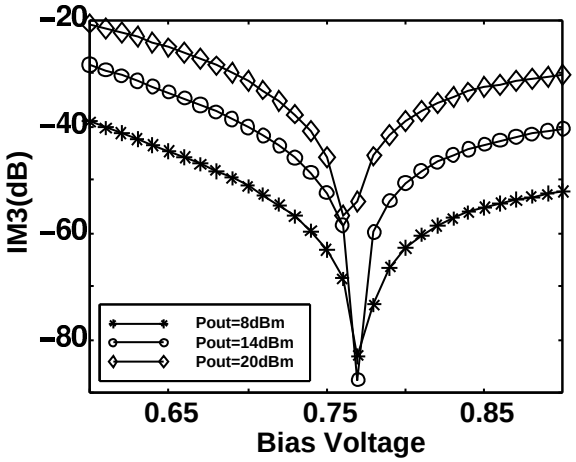

Fig. 3. Calculated IM3 with different bias voltages from (4)

III. Nonlinear Transconductance Analysis

The second source of nonlinearity is the nonlinear drain current, as shown in Fig. 1. During Class AB operation, the drain current is switched on and off, thus making the large-signal transconductance a highly nonlinear function of the gate voltage V_{gs} . Class AB operation is intrinsically very nonlinear. Our approach is to approximate the current(for a finite range of input) by a high order polynomial:

$$I_d = G_0 + G_1(V_{gs} - V_{bias}) + G_2(V_{gs} - V_{bias})^2 + ... + G_7(V_{gs} - V_{bias})^7 + \text{Fit Error} \tag{4}$$

We can calculate the third-order intermodulation(IM3) from the odd-order coefficients, i.e. G_3, G_5, G_7.... For different bias voltages, the polynomials are different, then we are able to decide which bias is best in terms of transconductance linearity. For Class B bias, all the high odd terms of the fitting polynomial are zero, which implies that IM3 is zero. Fig. 3 shows the theoretically calculated IM3 versus different gate bias voltages. The linearity measurements verify our analysis.

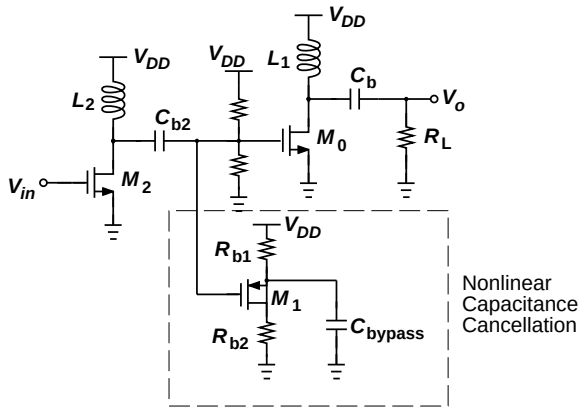

Fig. 4. Schematic of the two-stage Class AB power amplifier

IV. Simulation and Experimental Results

In order to verify this technique, we designed a two-stage $0.6\mu m$ CMOS Class AB power amplifier with nonlinear capacitor compensation and bias optimization. The amplifier operates at 1.9GHz PCS band, and is designed to deliver 100mW output power to a 50 Ohm load from a single 3.3V supply. The amplifier is highly integrated in the sense that the driver stage and inter-stage matching are all on chip. For the purpose of keeping good linearity, the driver stage is designed as a linear Class A amplifier.

The circuit schematic is shown in Fig. 4 and the die photograph is shown in Fig. 5. To minimize die area, we use Poly-Nfield capacitor and salicided polysilicon resistors provided by the process, and design a multi-layer octagonal on-chip inductor, which has a Q of approximately 5. The two NMOS transistors and the PMOS transistor comprise arrays of $20\mu m$ wide unit transistors. Wide metal lines are used for drain and source of the output transistors to reduce the parasitic resistance and increase current handling capability. The simulated maximum drain efficiency is approximately 50% for the output stage, and 40% for the entire two-stage amplifier. The two-tone

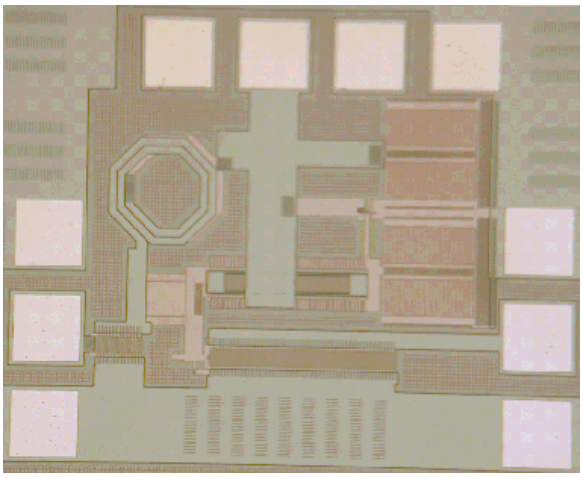

Fig. 5. Die photo of the amplifier with nonlinear cancellation circuitry

SPICE simulation shows that at the maximum single-tone power level, the circuit with compensation has about 8 dB improvement in its third-order intermodulation compared to the original Class AB NMOS amplifier.

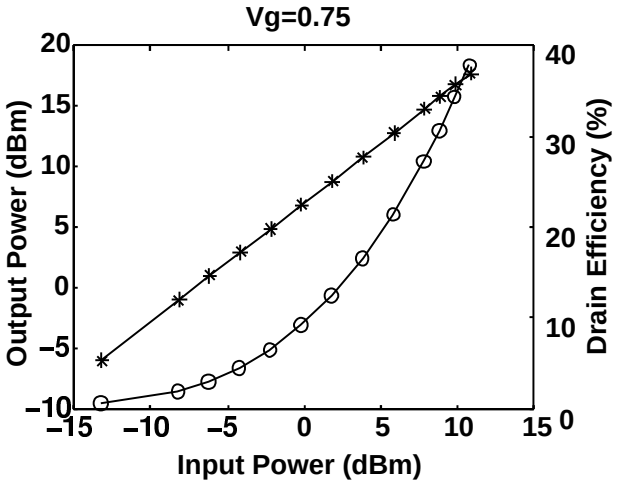

Fig. 6. Measured output power and efficiency for single-stage amplifier

For different gate biases, we achieve approximately $9.1 - 11.1dB$ gain for the single-stage amplifier without the capacitance compensation. With compensation, the power gain drops approximate 2dB. We achieve $15 - 18.5dB$ power gain for the entire two stage circuit. Fig. 6 shows the measured output power and drain efficiency for the output stage at the gate bias of 0.75V measured in a 50

Ohm environment.

Two-tone IM_3 measurement and CDMA IS95 Adjacent Channel Power Ratio(ACPR) measurement are made to evaluate the linearity of the amplifiers. Measurement data shows that the amplifier with nonlinear input capacitance compensation has at least $6dB$ IM_3 improvement in a wide range of output powers compared with the original amplifier without compensation, as shown in Fig. 7. Note that the P_{out} of the plot is the corresponding single-tone output power.

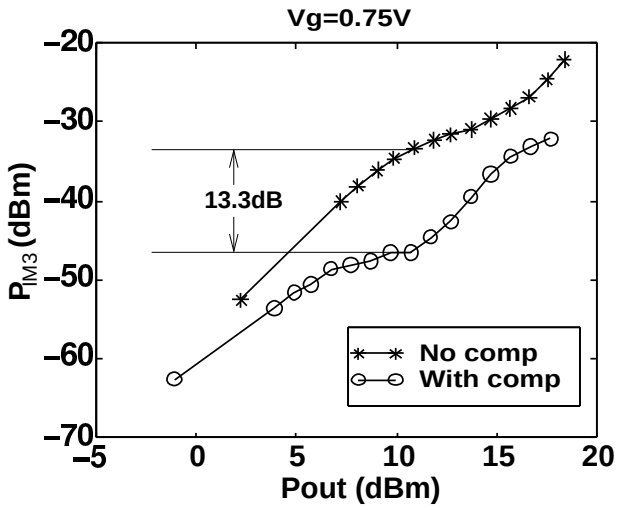

Fig. 7. Two-tone IM3 measurement results for amplifiers with and without nonlinear cancellation

Fig. 8 shows the measured output sprectrum of the amplifier with CDMA IS95 signal. The data shows that the amplifier with nonlinear capacitor cancellation has about $6dB$ lower sideband regrowth than the original amplifier at the same output power level.

V. Conclusions

The nonlinearity sources of NMOS ClassAB amplifiers are addressed and analyzed. In order to improve the linearity performance of NMOS Class AB power amplifiers, a nonlinear capacitance compensation technique is proposed, analyzed, simulated and implemented. According to simulation and experiemental results, the amplifier with the nonlinear compensation circuitry has improved linearity. The measured results also demonstrate the feasibility of linear CMOS power amplifier for RF wireless applications.

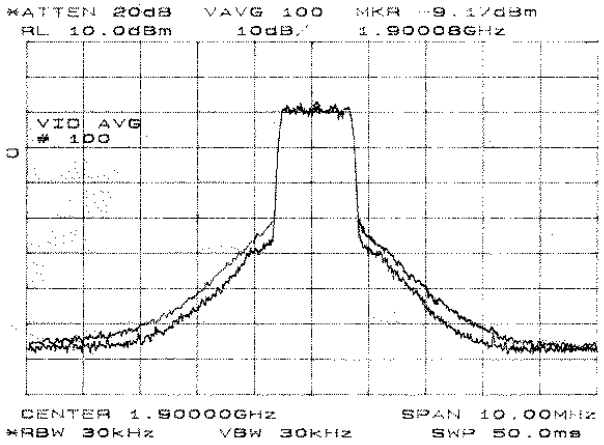

Fig. 8. Measured Class AB output spectra for CDMA IS95 with and without nonlinear cancellation

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